CLAIMS:

1. A method of debugging a target system using a host system connected thereto, the target system comprising a digital signal processor having associated memory comprising plural addressable locations, said target system further having a reserved storage location designated as a vector, said memory further storing plural application programs, each application program having respective associated exception handler code, the method comprising:

dynamically loading an stack to said reserved region;

causing the vector of said target system to point to said stack whereby all said applications use the said stack for said exception.

2. The method of claim 1 further comprising the steps of: -

dynamically loading a library to said target from said host whereby said dynamically loaded library has an entry point at one of said plural addressable locations, wherein said library includes at least one routine needed for running at least one of said applications; and

storing information indicative of the address of said one location at a reserved location in said stack.

3. The method of claim 2 further comprising the step of: -

using said host to start of one of said applications, whereby a running application identifies the need for said routine;

reading said vector;

using the contents of the vector to access said stack;

reading said reserved stack location to derive the entry point of said library to said application;

calling said routine from said library.

4. The method of claim 3 wherein said routine comprises a communication routine enabling said host and target to communicate.

5. The method of claim 3 wherein said routine comprises a routine enabling a hardware bug to be worked round.

6. The method of claim 3 wherein said step of calling comprises supplying a first item of data indicative of the routine and a second item of data for the operation to be performed by said routine.

7. The method of claim 6 wherein said routine returns an item of data to said application.

8. The method of claim 6 wherein each said data item comprises a machine word.

9. A device for debugging a target system, the device comprising a host system connected thereto, the target system comprising a digital signal processor having associated memory comprising plural addressable locations, said target system further having a reserved storage location designated as a vector, said memory further storing plural application programs, each application program having respective associated exception handler code, the device further comprising:

stack dynamic loading circuitry in said host for dynamically loading a stack to said reserved region, whereby said loader comprises an indication of the location in said memory of said stack;

vector writing circuitry receiving said indication, and writing to said the vector of said target system the

address of said stack whereby all said applications use the said stack for said exception.

10. The device of claim 9 further comprising: -

a computer file in said host, said file comprising a library having a routine needed by at least one of said applications;

library dynamic loading circuitry for dynamically loading said library to said target from said host whereby said dynamically loaded library has an entry point at one of said plural addressable locations; and

stack writing circuitry for storing information indicative of the address of said one location at a reserved location in said stack.

11. The device of claim 10 further comprising: -
control circuitry in said host for starting one of said applications, whereby a running application identifies the need for said routine;
vector reading circuitry in said target for reading the content of said vector;
addressing circuitry for using the contents of the vector to access said stack;
stack reading circuitry for reading said reserved stack location to derive the entry point of said library to said application;
calling circuitry for calling said routine from said library.

12. The device of claim 11 wherein said calling circuitry is operable to supply a first item of data indicative of the routine and a second item of data for the operation to be performed by said routine.

13. The device of claim 12 wherein each said data item comprises a machine word.